

BL6523B Application Note

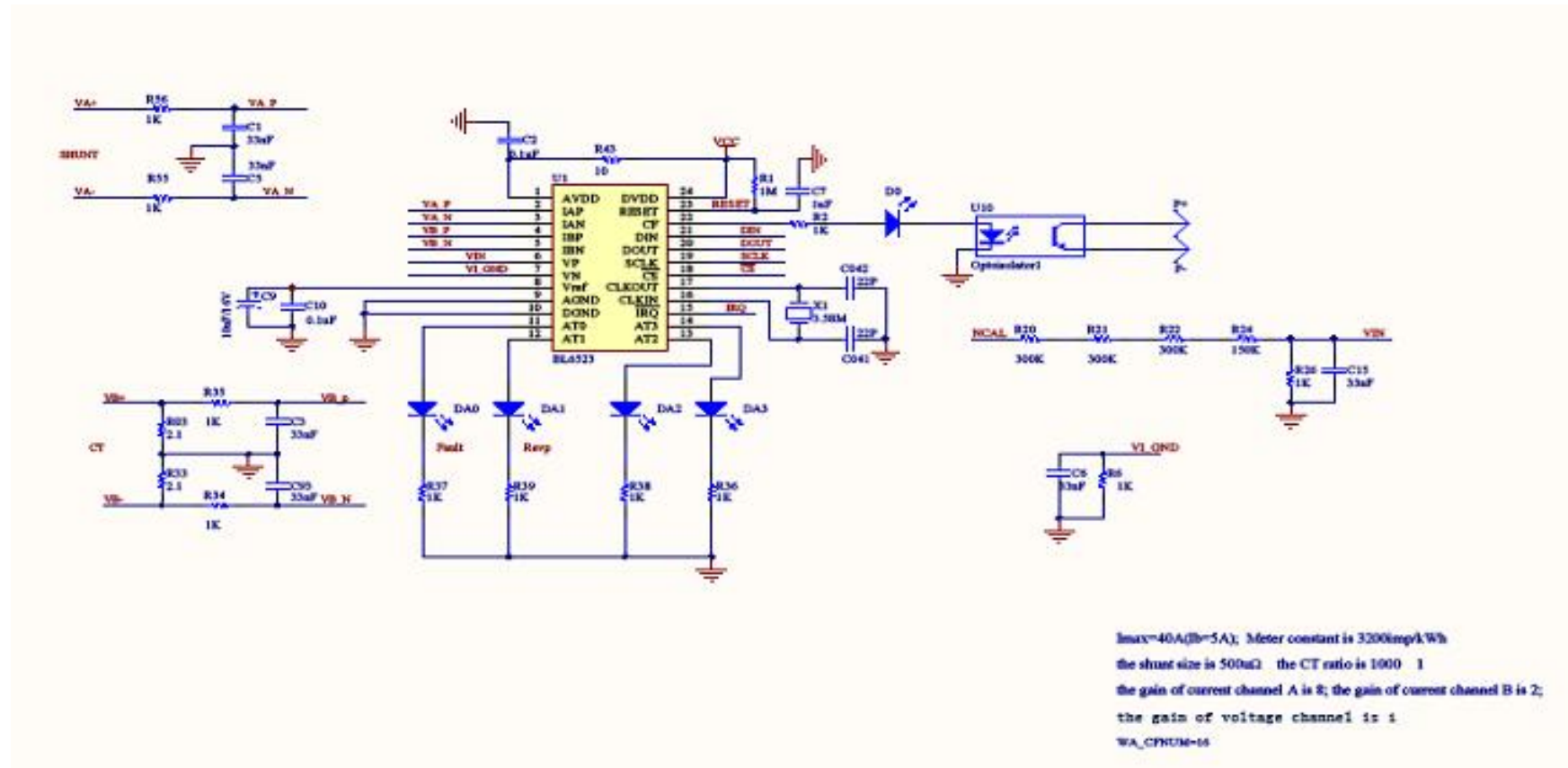
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BL6523B FEATURE

- ✿ High accuracy, less than 0.1% error over a dynamic range of 3000:1
- ✿ High stability, less than 0.1% error in the output frequency fluctuation
- ✿ Measure the active power in the positive orientation and negative orientation, transform to fast pulse output(CF)
- ✿ Provide two current input for line and neutral current measurement
- ✿ Measure instantaneous IRMS and VRMS over a dynamic range of 1000:1
- ✿ Provide SAG detection and Phase failure detection
- ✿ On-chip power supply detector
- ✿ On-chip anti-creep protection with the programmable threshold set
- ✿ Provide the pulse output with programmable frequency adjustment
- ✿ Provide the programmable gain adjustment and phase compensation
- ✿ Measure the power factor (PF)
- ✿ Provide a programmable interrupt request signal (/IRQ)
- ✿ Provide a SPI communication interface
- ✿ On-chip voltage reference of 2.5V
- ✿ With 3.58MHz external crystal oscillator
- ✿ Single 5V supply, 25mW (typical)

BL6523B typical test circuit



BL6523B SPI communication

SPI operation caution

1. The serial peripheral interface of the BL6523B uses four communication pins: /CS, SCLK, DIN, DOUT. The SPI communication operates in slave mode, a clock must be provided on the SCLK pin. This clock synchronizes all communication. The DIN pin is an input to the BL6523B; data is sampled by BL6523B on the rising edge of SCLK. The DOUT pin is an output from the BL6523B; data is shifted out on the rising edge of SCLK. The /CS (chip select) input must be driven low to initialize the communication and driven high at the end of the communication. Driving the /CS input high before the completion of a data transfer ends the communication.
2. The SPI communication packet consists of an initial byte. The Bit [7:6] of this byte dictates whether a read or a write is being issued. The Bit [7:6] of this byte should be set to 00 for a read operation and to 01 for a write operation. The Bit [5:0] of this byte is the address of the register that is to be read from or written to. This byte should be transmitted MSB first.

The bit count of a R/W operation is 32Bit, one initial byte (8Bit) +three data bytes(24Bit) ; if the data of the register is less than 24Bit, then fill 0 in front of the data to 24Bit.

In read operation, the initial byte is:

0	R/W=0	D5	D4	D3	D2	D1	D0
---	-------	----	----	----	----	----	----

D5~D0:the address of the register;

In write operation, the initial byte is

0	R/W=1	D5	D4	D3	D2	D1	D0
---	-------	----	----	----	----	----	----

D5~D0:the address of the register;

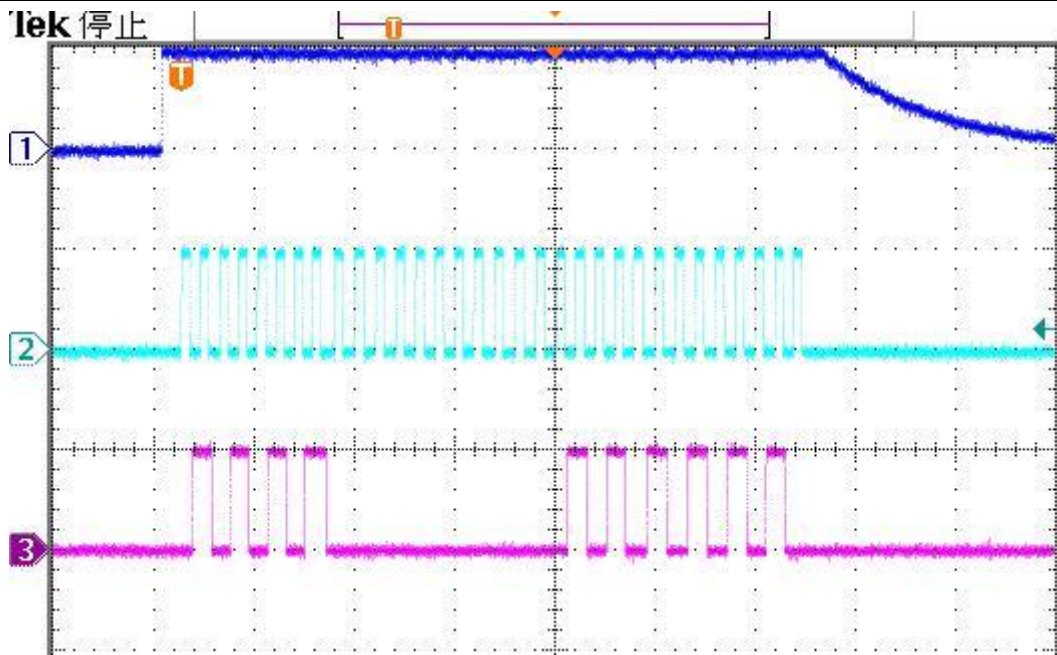
Three data(24Bit)

Highest byte(8Bit)	Middle byte(8Bit)	Lowest byte(8Bit)
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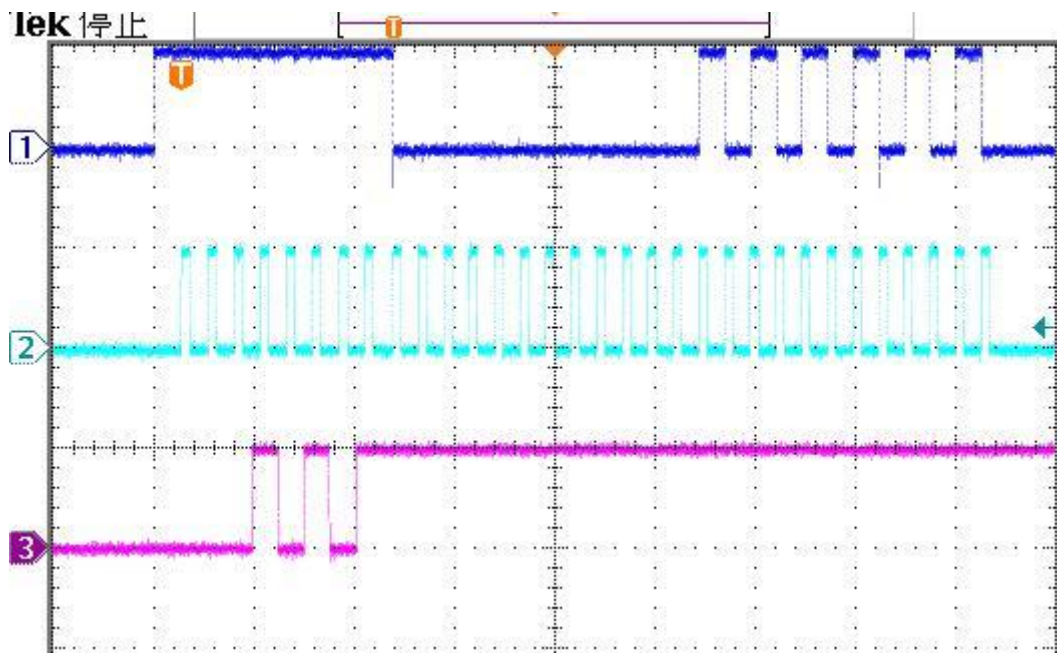
3. Before the signal of /CS is driven low, please make sure the signal of SCLK, DIN are low level.

Typical SPI timing diagram to read and write

Example: write register 15H, the writing value is AAAH



Waveform 1 for DOUT, Waveform 2 for SCLK. Waveform 3 for DIN;
Example : read register 15H, the reading value is AAAH



Waveform 1 for DOUT, Waveform 2 for SCLK. Waveform 3 for DIN;

The program of reading and writing

```
void SPI_Read(u8 Cmd)
    //SPI Read data
{
    s8 n,m;
```

```

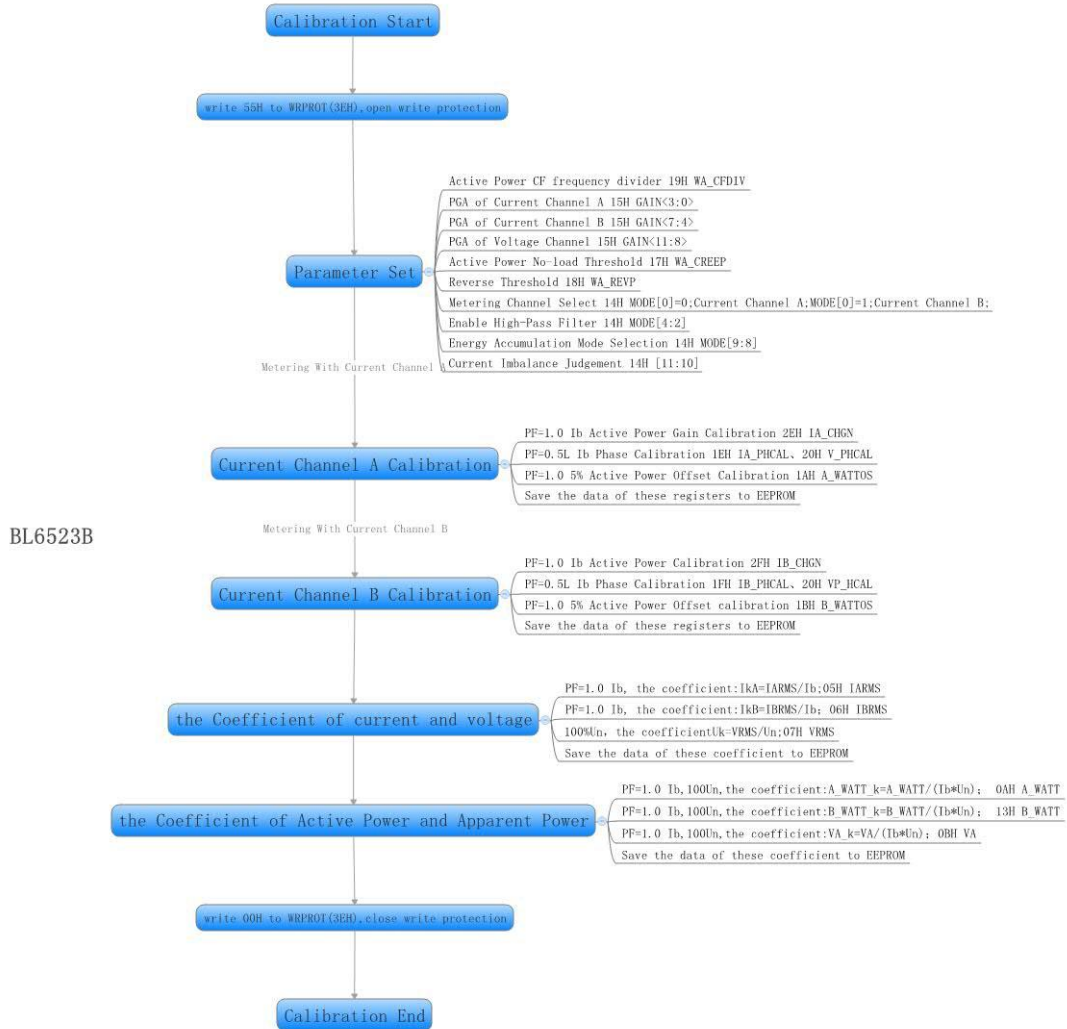
GPIO_WriteHigh(SPI_PORT,SPI_CS);           //CS=1
Delay(2);
GPIO_WriteLow(SPI_PORT,SPI_SCLK);          //SCLK=0
Delay(2);
GPIO_WriteLow(SPI_PORT,SPI_CS);           //CS=0
Delay(2);
//send CMD byte
for(n=7;n>=0;n--)
{
    GPIO_WriteLow(SPI_PORT,SPI_SCLK);      //SCLK=0
    Delay(2);
    if(ValBit(Cmd,n)==0)                    //MCU send the data to DIN pin
        GPIO_WriteLow(SPI_PORT,SPI_DIN);
    else
        GPIO_WriteHigh(SPI_PORT,SPI_DIN);
    Delay(2);
    //SCLK=1;the data is shifted in the BL6523B on the rising edge of SCLK
    GPIO_WriteHigh(SPI_PORT,SPI_SCLK);
    Delay(2);
}
GPIO_WriteLow(SPI_PORT,SPI_SCLK);          //SCLK=0
Delay(18);
//output three bytes from the DOUT pin of the BL6523B
for(m=2;m>=0;m--)
{
    for(n=7;n>=0;n--)
    {
        GPIO_WriteHigh(SPI_PORT,SPI_SCLK); //SCLK=1
        Delay(2);
        GPIO_WriteLow(SPI_PORT,SPI_SCLK);  //SCLK=0
        Delay(2);
        //MCU get data from DOUT pin
        BL6523B_Data_Read[m]=BL6523B_Data_Read[m]<<1;
        if(GPIO_ReadInputPin(SPI_PORT,SPI_DOUT))
            BL6523B_Data_Read[m]=BL6523B_Data_Read[m]+1;
        Delay(2);
    }
}
GPIO_WriteHigh(SPI_PORT,SPI_CS);           //CS=0, end SPI
Delay(2);
GPIO_WriteLow(SPI_PORT,SPI_SCLK);          //SCLK=0
}

```

```

void SPI_Write(u8 Cmd)
{
    s8 n,m;
    //write operatin, the bit[7:6] of the cmd byte should be 01
    Cmd=Cmd|0x40;
    GPIO_WriteHigh(SPI_PORT,SPI_CS);           //CS=1
    Delay(2);
    GPIO_WriteLow(SPI_PORT,SPI_SCLK);         //SCLK=0
    Delay(2);
    GPIO_WriteLow(SPI_PORT,SPI_CS);           //CS=0
    Delay(2);
    for(n=7;n>=0;n--)
    {
        GPIO_WriteLow(SPI_PORT,SPI_SCLK);     //SCLK=0
        if(ValBit(Cmd,n)==0)
            GPIO_WriteLow(SPI_PORT,SPI_DIN);
        else
            GPIO_WriteHigh(SPI_PORT,SPI_DIN);
        Delay(2);
        //SCLK=1;the data is shiftedin the BL6523B on the rising edge of SCLK
        GPIO_WriteHigh(SPI_PORT,SPI_SCLK);
        Delay(2);
    }
    GPIO_WriteLow(SPI_PORT,SPI_SCLK);         //SCLK=0
    for(m=2;m>=0;m--)
    {
        for(n=7;n>=0;n--)
        {
            GPIO_WriteLow(SPI_PORT,SPI_SCLK); //SCLK=0
            if((BL6523B_Data_Write[m]&((u8)1<<n))==0)
                GPIO_WriteLow(SPI_PORT,SPI_DIN);
            else
                GPIO_WriteHigh(SPI_PORT,SPI_DIN);
            Delay(2);
            //SCLK=1;the data is shiftedin the BL6523B on the rising edge of SCLK
            GPIO_WriteHigh(SPI_PORT,SPI_SCLK);
            Delay(2);
        }
    }
    GPIO_WriteLow(SPI_PORT,SPI_SCLK);         //SCLK=0
    Delay(18);
    GPIO_WriteHigh(SPI_PORT,SPI_CS);           //CS=1, end SPI
}
    
```

BL6523B calibration process



Special registers

The BL6523B contains Write protection register (WRPROT), the default value of the WRPROT register is 00H, write disable. Before writing operation to calibration register, the WRPROT register must set to 55H through SPI, open the write-protect, the data can be written successfully. Otherwise it is impossible to write in. After completion of calibration registers setting, the WRPROT register is written any value except 55H, close the write-protect, all data can't be written to BL6523B.

The READ register contains the data from the last read operation of SPI. The WRITE register contains the data from the last write operation of SPI. The user can program the SPI communication redundancy to ensure the reliability of SPI communication.

The CHKSUM register contains the sum of calibration register. the user can check whether this register value changes to determine whether the error occur in the BL6523B.

Active power CF frequency divider (WA_CFDIV 19H)

D11	D10	D9	D8	D3	D2	D1	D0
-----	-----	----	----	-------	----	----	----	----

This register set the CF Pulse frequency.

At maximum signal level $\pm 660\text{mV}$ (467mV rms)				
Typical value				
CFDIV register(30H)	The frequency of CF (Hz)	WATT register	IA_RMS register	V_RMS register
1(001H)	1.95	6500000	5650000	5650000
2(002H)	3.91			
4(004H)	7.81			
8(008H)	15.63			
16(010H)	31.25			
32(020H)	62.50			
64(040H)	125.00			
128(080H)	250.00			
256(0100H)	500.00			

MODE register(MODE 14H)

D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
-----	-----	----	----	----	----	----	----	----	----	----	----

- D0 0, metering with current channel A; 1, metering with current channel B.
- D1 Reserved;
- D4~D2 High-pass filter selection. The default value is 000, enable high-pass filter.
 - D2=0, enable the high-pass filter of current channel A,
 - D2=1, disable the high-pass filter of current channel A.
 - D3=0, enable the high-pass filter of current channel B
 - D3=1, disable the high-pass filter of current channel A.
 - D4=0, enable the high-pass filter of voltage channel.
 - D4=1, disable the high-pass filter of voltage channel.
- D7 **D7 must be set to 1.**
- D9~D8 Energy accumulation mode selection.
 - 00, absolute energy accumulation mode. (default)
 - 01, positive-only energy accumulation mode.
- D11~D10 the current imbalance threshold.

D[11]	D[10]	Threshold
0	0	12.5%(default)
0	1	6.25%
1	0	3.125%
1	1	10.1%

Example: 220V AC, absolute energy accumulation mode, measuring energy at channel A, the MODE register will be set to 080H.

Gain register (GAIN 15H)

Gain of voltage channel				Gain of current channel B				Gain of current channel A			
x	D10	D9	D8	x	D6	D5	D4	x	D2	D1	D0

Every analog channel has a programmable gain amplifier. Every 4-bit of the gain register used to select the current channel or voltage channel PGA. Gain[3:0] used to select Current A channel PGA, Gain[7:4] used to select Current B channel PGA, Gain[11:8] used to select Voltage channel PGA. The PGA can be set to 1, 2, 4, 8, 16, 24, 32;

For example Gain [3:0]:

$$x000 = 1x$$

$$x001 = 2x$$

$$x010 = 4x$$

$$x011 = 8x$$

$$x100 = 16x$$

$$x101 = 24x$$

$$x110 = 32x$$

Example: Assume the PGA of channel voltage is 1, the PGA of current channel A is 16, the PGA of current channel B is 1, the gain register will be set to 004H.

No-load threshold of active power(WA_CREEP 17H)

Active Power Noload threshold(WA_CREEP) Addr: 17H				Type: R/W	Default: FFF02BH	
Bit23	Bit22	Bit21	...	Bit14	Bit13	Bit12
Bit11	Bit10	Bit9	...	Bit2	Bit1	Bit0

Bit[23:12] is used to set time-creep threshold. 1LSB=4.6 second.

Bit[11:0] is used to set active power noload threshold. When the absolute value of the input power signal is less than this threshold, the output active power is set to zero. This can make in no-load conditions, even a small noise signal output to the active register is 0.

One LSB in the WA_CREEP [11:0] register is equivalent to 0.366 LSBs in the WATT register.

Example: the value of WATT register is 249F0H (150000) (100%Un, 100%Ib), the starting current of the meter is 0.4%Ib. the No-Load threshold value of active power can be set to 0.2%Ib*Un. (150000*0.2%=300), the value of WA_CREEP[11:0] is 300*0.366≈110(6EH)

Reverse indicator threshold (WA_REVP 18H)

D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
-----	-----	----	----	----	----	----	----	----	----	----	----

this register is in 12-bit unsigned magnitude format, When the input power signal is negative and the absolute value is greater than the power threshold, the BL6523A output the REVP indicator.

One LSB in the WA_REVP register is equivalent to 0.0229 LSBs in the WATT register.

Example: the value of WATT register is 249F0H (150000) (100%Un, 100%Ib), the reverse indicator should be work when the current larger than 0.4%Ib. the threshold register of reverse

indicator(WA_REVP 18H) can be set to $0.4\%I_b \cdot U_n \cdot 0.0229 = 150000 \cdot 0.4\% \cdot 0.0229 \approx 14(0EH)$

Current imbalance shielding threshold (FAULTLVL 16H)

D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
-----	-----	----	----	----	----	----	----	----	----	----	----

This register ia in 12-bit unsigned magnitude format, when the rms value of the current is less than this threshold, the BL6523B will close the current imbalance detection.

Example : close the detection of current imbalance when the value of IA_RMS register less than 10000(2710H), the FAULTLVL register should be set $10000/256=39(027H)$

If the design of the meter does not require the detection of current imbalance, this register keep the default value.

Active power calibration

1. Gain calibration in Ib

Test condition: 100%Un, 1.0, Err: percentage error of active power accuracy.

$$\text{If } Err < 0, \text{ then } WATTGN = 2^{12} \times \frac{-Err}{1 + Err}$$

$$\text{If } Err \geq 0, \text{ then } WATTGN = 2^{12} + 2^{12} \times \frac{-Err}{1 + Err}$$

Calibration registers:

2EH current A channel gain adjustment register IA_CHGN;

2FH current B channel gain adjustment register IB_CHGN;

The Err can be calibrated when the active power initial error range is -33.3%~+99.9%

12 bits register, Complement form.

2. Phase calibration in Ib 0.5 inductive (Ib 0.5L)

Enable bit											
D7	D6	D5	D4	D3	D2	D1	D0				

D7 is enable bit, =1, enable phase compensation, =0, disable phase compensation.

Test condition: Ib, PF=0.5L, the frequency is 50Hz. Assume the error from the calibration bench is Err.

$$\theta \approx \arcsin\left(\frac{|Err|}{1.732}\right)$$

phase calibration is

$$PHCAL = (\text{int}(\theta/0.02-1)) |0x80;$$

If Err ≥ 0, the PHCAL is written to IA_PHCAL, IB_PHCAL;

If Err < 0, the PHCAL is written to V_PHCAL;

1EH phase calibration register (current channel A); IA_PHCAL; the maximum

value is 255, FFH, 2.54°

- 1FH phase calibration register (current channel B); IB_PHACL;
- 20H phase calibration register (voltage channel); V_PHCAL;
- 1LSB of register may cause the Err change 0.0605%.

3. Active energy offset calibration

Active energy offset calibration is only required if accuracy of active power at low loads is 小电 outside the required specification prior to offset calibration

- 1AH active power offset correction (current channel A) A_WATTOS;
- 1BH active power offset correction (current channel B) B_WATTOS;

12 Bits register, complement form.

Assume at low loads, the value of X_WATT register is WATT_Data, the percentage error of active power accuracy is Err, then $X_WATTOS = \frac{WATT_Data * (-Err)}{(1+Err) * 1.3655}$

Example: at 5%I_b current, 100%U_n, X_WATT=2710H(10000), Err=0.45%, then $X_WATTOS = \frac{10000 * (-0.0045)}{(1+0.0045) * 1.3655} = -33 = FDFH(4063)$

4. Current RMS adjustment

At 100%U_n, I_b 1.0, the value of IARMS register is IARMS_I_b, the transfer coefficient of current A is I_{kA} = $\frac{IARMS_Ib}{Ib}$; then the current value at any load is $\frac{IARMS}{IKA}$

The transfer coefficient of current B can be get in the same way.

- 05h Irms register(Channel A) IARMS;
- 06h Irms register(Channel B) IBRMS;

5. Voltage RMS adjustment

At 100%U_n, the value of VRMS register is VRMS_U_n, the transfer coefficient of voltage is 在

$$U_k = \frac{VRMS_Un}{Un}$$

- 07h vrms register V_RMS;

6. Line voltage frequency FREQ (09H)

At frequency 50Hz, the value of FREQ register is FREQ_50, the transfer coefficient of FREQ is K_f = 50 * FREQ_50;

When frequency changed, the measured frequency is $f = \frac{Kf}{FREQ}$

- 09H frequency register FREQ

7. Power factor register PF (08H)

D23	D22	D21	...	D3	D2	D1	D0
-----	-----	-----	-----	----	----	----	----

D23 is the sign bit;

$$PF = 2^{-1} * D22 + 2^{-2} * D21 + 2^{-3} * D20 + \dots + 2^{-21} * D2 + 2^{-22} * D1 + 2^{-23} * D0$$

PF=active power/(IRMS*URMS);

8. Active power register (0AH A_WATT Average active power of channel A; 13H B_WATT Average active power of channel B)

24 bits register, complement form.

Assume at 100%Un, Ib 1.0, the active power is P, the value of X_WATT is WATT_Data, then the transfer coefficient of WATT is:

If $WATT_Data \leq 2^{23}$, $Watt_K = P / WATT_Data$;

If $WATT_Data > 2^{23}$, $Watt_K = P / (WATT_Data - 2^{24})$;

9. Apparent power register VA (0BH)

24 bits register.

Assume at 100%Un, Ib 1.0, the apparent power is S, the value of VA is VA_Data, then the transfer coefficient of VA is :

$VA_K = S / VA_Data$;

Design Guide

Example:

Assume Un=220V, Ib=10A, I_{max}=60A, Meter Constant: 1600imp/kWh.

1. The voltage divider coefficient=800, so $V_U = 220V / 800 = 275mV$.
2. L line shunt resistor=250μΩ, At I_{max}(60A) current, the sample signal of current channel is 60A*250μΩ =15mV rms; So the PGA of current channel is 16.

Current channel PGA	Maximum input signal (peak-peak)	Maximum input signal (RMS)
1	± 660mV	467mV
2	± 330mV	233mV
...
16	± 41.3mV	29.2mV
24	± 27.5mV	19.45mV
32	± 20.63mV	14.6mV

3. The value of WA_CFDIV

At maximum signal level ±660mV (467mV rms)				
	Typical value			
WA_CFDIV	The frequency of CF (Hz)	WATT register	IA_RMS register	V_RMS register
1(0x01)	1.95	6500000	5650000	5650000
2(0x02)	3.91			
4(0x04)	7.81			
8(0x08)	15.63			
16(0x10)	31.25			
32(0x20)	62.50			
64(0x40)	125.00			
128(0x80)	250.00			
256(0x100)	500.00			

The constant of meter is 1600imp/kWh,
At 100% U_n , I_{max} 1.0
The frequency of CF output $= (220V * 60A * 1600) / (3600 * 1000) = 5.87Hz$;
the signal of voltage channel is 275mV rms, the PGA of voltage channel is 1;
the signal of current channel is 15mV rms, the PGA of current channel is 16;
so the frequency of CF output at full scale signal input both current and voltage
channel is $5.87 * 467 * 467 / (275 * 15 * 16) = 19.4Hz$.
From the above table, WA_CFDIV can choose 8. Because the frequency of CF at
WA_CFDIV=8 is the most close to 19.4Hz.

4. The creep of active power
See “BL6523B calibration process” section
5. Meter calibration
See “BL6523B calibration process” section